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AMENDMENTS TO THE SPECIFICATION

Please amend the specification as indicated hereafter. It is believed that the following amendments and additions add no new matter to the present application.

In the Specification: [Use strikethrough for deleted matter (or double square brackets "[[]]" if the strikethrough is not easily perceivable, *i.e.*, "4" or a punctuation mark) and <u>underlined</u> for added matter.]

Please amend the paragraph starting on p. 2, line 27 as follows:

Several variations of new multiple channel DSL technology exist, such as, but not limited to, Asymmetric Digital Subscriber Line (ADSL), Rate Adaptive Digital Subscriber Line (RADSL), Very High Speed DSL (VDSL), Multiple Virtual Lines (MVLTM) and TripleplayTM, with this group generally referred to as xDSL. Communication systems carrying xDSL may multiplex xDSL signals and a POTS signal onto a single physical local loop. Typically, an individual subscriber loop consists of two copper wires insulated from each other and bound together either in a common wire bundle of a plurality of subscriber loops or bound together into a single cable. For convenience, subscriber loops residing in the CP have been traditionally made with two subscriber loops, that is four copper conductors, bound together into a single four wire cable which is run throughout the customer premises to provide POTS telephony service. Also, 3-pair wires are very common, with the third pair seldom used. These four conductors may or may not be twisted together when formed into a single cable.

Please amend the paragraph starting on p. 8, line 5 as follows:

In the simplified illustrative example of FIG. 1, two subscriber loops 126 and 128 are shown to provide connection to digital devices 152 and 162 to the central office digital equipment 158 and 164, respectively. When the four electrical conductors, line 1, line 2, line 3 and line 4, are bundled together, each line will be capacitively coupled to some degree with each of the other lines. The degree of capacitive coupling will be, in part, a function of the proximity of each electrical conductor with the other electrical conductors. Thus, line 1 will be capacitively [[y]] coupled to line 2 by C12 (using the nomenclature as described above for C12), capacitively

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coupled with line 3 through C13, and capacitively coupled with line 4 through C14. Here, C12 also represents the capacitive coupling of line 2 with line 1. C13 also represents the capacitive coupling of line 3 with line 1 (FIG. 1) and, C14 also represents the capacitive coupling of line 4 with line 1. Line 2 is capacitively coupled to line 3 and line 4 of subscriber loop 126 through C23 and C24, respectively.

Please amend the paragraph starting on p. 10, line 23 as follows:

The preferred embodiment of the crosstalk compensator has two groups, each group having three compensating capacitors. The compensating capacitors have switches such that, when connected in parallel with two subscriber loops that have a mismatch in their mutual coupling capacitances, one of or more of the compensating capacitors may be connected such that the mismatch is reduced or eliminated, thereby reducing or eliminating the undesirable PEXT interference.



FIG. 11 illustrates a fifth alternative embodiment of the crosstalk compensator 205. This fifth alternative embodiment of the crosstalk compensator 205 is similar to the fourth alternative embodiment of the crosstalk compensator 204 (FIG. 10) in that the crosstalk compensator 205 has the line switching functions and the compensating capacitor switching functions controlled by a processor 272 which controls line switcher 274 and CC switcher 276. Processor 272, line switcher 274 and CC switcher 276 are substantially similar to the processor 262, line switcher 264 and CC switcher 266 (FIG. 9). However, this alternative embodiment of the crosstalk compensator 205 shown in FIG. 11 contains a detector 278 as part of the processor based detector and switch 270. With this alternative embodiment, the installer would merely connect the crosstalk compensator 205 to line 1, line 2, line 3 and line 4 as shown in FIG. 11. The detector 278 would then detect the presence of any mismatch in mutual coupling capacitance C13, C14, C23 and/or C24 (FIG. 5) and communicate the mismatch information to the processor 272. Processor 272 would analyze the detected mismatches to determine whether an undesirable significant level of PEXT interference would be present. Processor 272 would then determine the amount of required compensating capacitance to mitigate the identified greatest mismatch

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and determine the appropriate switch connections for the line switches residing in line switcher 274 and the compensating capacitor switches residing in CC switcher 276. Then, the processor 272 would instruct line switcher 274 and CC switcher 276 to connect compensating capacitor group CCX to the appropriate conductors of subscriber lines 126 and 128 such that the PEXT interference caused by the identified greatest mismatch is mitigated. With this alternative embodiment of a crosstalk compensator 205, the single compensating capacitance CCX could only be used to compensate a single mismatch in the above-described mutual coupling capacitance.

Please amend the paragraph starting on p. 31, line 11 as follows:

XI. Method for Sixth An Alternative Embodiment

FIG. 14 is a flow chart 320 illustrating the logic residing in processor 302 of crosstalk compensator 207 (FIG. 13). The flow chart of FIG. 14 shows the architecture, functionality, and operation of a possible implementation of the software for implementing the logic residing in processor 302. In this regard, each block may represent a module, segment or portion of code, which comprises one or more executable instructions for implementing the specified logical function(s). It should also be noted that in some alternative implementations, the functions noted in the blocks may occur out of the order noted in FIG. 14 or may include additional functions without departing significantly from the functionality of the crosstalk compensator 207. For example, two blocks shown in succession in FIG. 14 may in fact be executed substantially concurrently, the blocks may sometimes be executed in the reverse order, or some of the blocks may not be executed in all instances, depending upon the functionality involved, as will be further clarified hereinbelow.

